IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1 and 6-9 in accordance with the following:

1. (CURRENTLY AMENDED) A method of forming a conductor wiring pattern, comprising:

forming a first insulating layer on a surface of a substrate and forming a second, photosensitive insulating resin layer thereon;

light-exposing and developing the second insulating layer to form pattern grooves, each having sidewalls and a bottom, so that the first insulating layer is exposed at the bottom of each pattern groove;

forming a plating seed layer on the second insulating layer including inner surfaces of the pattern grooves and then forming a resist pattern on the plating seed layer except for portions of the pattern grooves of the second insulating layer so that the plating seed layer only on the sidewalls and the bottom of the pattern groove is exposed;

filling the pattern grooves with a conductor having an upper surface by an electrolytic plating using the plating seed layer as a power supply layer;

coating the upper surface of the conductor with a barrier layer; and

removing the resist pattern and also removing by etching the plating seed layer exposed on the surface of the second insulating layer to form a wiring pattern consisting of ~~conductors~~ the conductor remaining in the pattern grooves, while the upper surface of the conductor filled in the pattern grooves is protected by the barrier layer.

2. (ORIGINAL) A method as set forth in claim 1, wherein a plurality of different metal layers are used, as the conductor, when the pattern grooves are filled with the conductor by the electrolytic plating.

3. (ORIGINAL) A method as set forth in claim 2, wherein the plurality of different metal layers are at least two metal layers consisting of a copper base layer and a nickel barrier layer.

4. (PREVIOUSLY PRESENTED) A method as set forth in claim 1, wherein:

the first insulating layer is composed of a photosensitive insulating resin; and

after the first insulating layer is light-exposed and developed to form an opening, through which a first wiring pattern formed on the substrate is to be electrically connected to a second wiring pattern to be formed on the first insulating layer, the first insulating layer is heated and hardened.

5. (ORIGINAL) A method as set forth in claim 1, wherein a semiconductor wafer is used as the substrate, the semiconductor wafer has an electrode terminal forming surface, on which the first insulating layer and the second insulating layer are formed, and the wiring pattern, which is electrically connected with electrode terminals of the semiconductor wafer, is formed.

6. (CURRENTLY AMENDED) A method of forming a conductor wiring pattern, comprising:

forming a first insulating layer on a surface of a substrate and forming a second, photosensitive insulating resin layer thereon;

light-exposing and developing the second insulating layer to form one or more conductor paths having inner surfaces sidewalls and a lowest horizontal surface, so that the first insulating layer is exposed at the lowest horizontal surface of each of said one or more conductor paths;

forming a plating seed layer on the second insulating layer including said one or more conductor paths having inner surfaces sidewalls and a lowest horizontal surface and then forming a resist pattern on the plating seed layer except for said inner surfaces sidewalls and a lowest horizontal surface of said one or more conductor paths so that the seed layer is exposed only on said inner surfaces sidewalls and a lowest horizontal surface of said one or more conductor paths;

filling ~~the pattern grooves~~said one or more conductor paths with a conductor having an upper surface by an electrolytic plating using the plating seed layer as a power supply layer;

coating the upper surface of the conductor with a barrier layer; and

removing the resist pattern and also removing by etching the plating seed layer exposed on the surface of the second insulating layer to form a wiring pattern consisting of ~~conductors~~ the conductor remaining in ~~the pattern grooves~~ said one or more conductor paths, while the upper surface of the conductor is protected by the barrier layer.

7. (CURRENTLY AMENDED) A method as set forth in claim 6, wherein said ~~step of~~ filling ~~the pattern grooves~~ said one or more conductor paths with a conductor comprises filling ~~the pattern grooves~~ said one or more conductor paths up to substantially the same thickness as that of the second insulating layer.

8. (CURRENTLY AMENDED) A method as set forth in claim 6, wherein said ~~step of~~ filling ~~the pattern grooves~~ said one or more conductor paths with a conductor comprises filling ~~the pattern grooves~~ said one or more conductor paths up to double the thickness of the second insulating layer.

9. (CURRENTLY AMENDED) A method as set forth in claim 6, wherein said ~~step of~~ removing the seed layer exposed on the surface of the second insulating layer comprises selectively removing portions of the seed layer on the surface of the second insulating layer so the conductor is protected by said inner surfaces defined by said sidewalls and a bottom of said one or more ~~pattern grooves~~ conductor paths and the second insulating layer of side portions from erosion.